ABSTRACT OF THE DISCLOSURE

In manufacturing a semiconductor memory, a gate oxide film, a polysilicon film and a WSi film are laminated on the major surface of a semiconductor wafer corresponding to both an element region on which a semiconductor chip is to be formed and a dicing region serving as a dicing line. These laminated films are patterned to form a projected dummy pattern having substantially the same wiring structure as that of a gate electrode portion of a selective transistor. The dummy pattern is formed between element isolation regions along a dicing direction at the same time when the gate electrode portion is formed. The dummy pattern prevents stress caused by dicing from being concentrated on an insulation film in the dicing region, thereby minimizing a crack waste. Consequently, in the semiconductor memory, a malfunction due to a large crack waste caused by the dicing, can be avoided.